

Aayush Kashyap

<http://thekingox9.github.io/>

kashyapaayush32@gmail.com | (+91) 836.848.1911

<http://linkedin.com/in/thekingox9>

EXPERIENCE

CADENCE | PRODUCT VALIDATION ENGINEER II

Sept 2025 – Present | Noida, India

- Validated mixed-signal and EM workflows across Virtuoso and Sigrity platforms to ensure production-ready tapeout flows.
- Analyzed simulation logs, crash dumps, and runtime traces to identify root causes in large-scale EDA software stacks.
- Developed automated validation scripts (Python, Bash, Make) to improve regression robustness and product coverage
- Collaborated with cross-functional engineering teams to resolve integration issues impacting customer design flows.

CADENCE | PRODUCT ENGINEERING INTERN

June 2025 – Sept 2025 | Noida, India

- Contributed to documentation of end-to-end RF and EM flow spanning schematic, layout, packaging, and PCB levels.
- Assisted in system-level integration verification across EMX, Clarity, Voltus-XFi, Microwave Office and Virtuoso.
- Worked with senior engineering teams to improve reliability of simulation workflows used in production design environments.

HASHSTASH | CONTRACT PROGRAMMER & GAME DEVELOPMENT INTERN

Apr 2022 - Sept 2022 & Apr 2021 – Aug 2021 | Noida, India

- Developed gameplay systems, integration pipeline, and prototypes for Android and HTML5 games.
- Collaborated with game designers and testers to ensure tight and bug-free gameplay mechanics.
- Supported performance profiling and iterative feature development under rapid delivery timelines.

EDUCATION

M.TECH. IN VLSI DESIGN | JAWAHARLAL NEHRU UNIVERSITY & IIT DELHI

May 2023 - May 2025 | New Delhi, India

B.TECH. IN ELECTRONICS AND COMMUNICATIONS ENGINEERING | JAWAHARLAL NEHRU UNIVERSITY

Oct 2020 - May 2025 | New Delhi, India

RELEVANT COURSEWORK:

Model Predictive Control • LQR and PID control • Semiconductor Memory Design • High Performance Computer Architecture • MOS VLSI Design • Digital Design Lab • Analog IC Design • Machine Learning • Control Systems

SKILLS

LANGUAGES: C • C++ • C# • Lua • Typescript • Python • Verilog • Makefile • Matlab • Bash

TECHNOLOGIES: FPGAs (Zynq UltraScale+) • RISC-V • Communication Protocols (I2C, SPI, UART) • Tensorflow • OpenCV • Git • Github • ROS • FreeRTOS • Linux Kernel • RaspberryPI • ESP32 • ESP-ADF • ESP-IDF • Alpine Linux • Ubuntu

TOOLS: PlatformIO • Cadence Tools (Virtuoso, Innovus, Genus, EMX, Clarity) • Quartus Prime • ModelSim, • Vivado • iVerilog • GHDL • XScem • ngspice • GTKWave • YoSYS

COURSES

ROBOTICS SPECIALIZATION | UNIVERSITY OF PENNSYLVANIA, COURSERA

NAND2TETRIS | HEBREW UNIVERSITY OF JERUSALEM, COURSERA

INTRODUCTION TO SELF-DRIVING CARS | UNIVERSITY OF TORONTO, COURSERA

PROJECTS (IMAGE PROCESSING)

REAL-TIME RADIATION DOSIMETRY USING RAW CAMERA SENSOR | M.TECH. DISSERTATION

- Designed a radiation sensing system using a RAW CMOS camera sensor interfaced to Raspberry Pi via CSI.
- Captured Bayer RAW frames by bypassing the default ISP to enable direct pixel-level signal analysis.
- Developed a custom image processing pipeline in Python (OpenCV) including: Demosaicing and denoising, event detection via adaptive thresholding and pixel clustering for radiation hit localization
- Modeled sensor noise characteristics and calibrated intensity-to-dose mapping for radiation estimation.
- Implemented near real-time dose computation on embedded Linux hardware.

3D POINT CLOUD RECONSTRUCTION FROM MULTI-ANGLE IMAGE DATA | ROBOTICS (PERCEPTION) COURSE

- Developed a MATLAB-based multi-view image processing pipeline to reconstruct 3D point clouds from images captured at multiple viewing angles.
- Implemented feature detection and correspondence matching across views.
- Applied camera projection geometry and triangulation to estimate spatial coordinates of scene points.
- Constructed 3D point maps and validated reconstruction accuracy using geometric error metrics.

PROJECTS (EMBEDDED SYSTEMS)

BLUETOOTH SPEAKER | FREELANCE

- Designed and implemented multithreaded firmware architecture across both ESP32 cores using FreeRTOS task scheduling, mutexes, and semaphores.
- Integrated A2DP Bluetooth audio streaming with external codec over I2S/I2C.
- Managed SPI-based LCD driver and SD card interface with concurrent access protection.
- Optimized power consumption using ESP32 ULP coprocessor and dynamic task management.

MOBILE INVERTED PENDULUM | ROBOTICS SPECIALIZATION CAPSTONE

- Modeled nonlinear dynamics and implemented Extended Kalman Filter (EKF) for state estimation.
- Designed real-time feedback control loop deployed on Arduino hardware platform.
- Integrated MPU6050 IMU and motor drivers with closed-loop stabilization.
- Achieved stable self-balancing operation under dynamic disturbances.

PROJECTS (CONTROL SYSTEMS AND ROBOTICS)

QUADCOPTER DYNAMICS AND PATH TRACKING | ROBOTICS SPECIALIZATION

- Modeled full 6-DOF quadcopter dynamics using Newton-Euler formalism, capturing translational and rotational coupling effects under near-hover conditions.
- Designed a nested control architecture with Inner-loop PID controllers for roll, pitch, and yaw stabilization and outer-loop position controller for altitude and planar motion tracking
- Developed piece-wise quadratic spline trajectory generator to produce smooth, differentiable 3D paths.
- Implemented feedforward + feedback control integration to reduce steady-state tracking error.

REMOTE INTERFACE FOR ROBOMUSE | INDIAN INSTITUTE OF TECHNOLOGY, DELHI

- Developed a remote control interface for RoboMuse5 to monitor resource usage and issue real-time commands, featuring a dynamic React frontend and Dart backend.
- Implemented a multithreaded control system where one thread managed the server and another interfaced with ROS via Dart bindings, using message passing for efficient real-time communication.

PROJECTS (VERILOG)

8-CORE GENERAL PURPOSE GRAPHICS PROCESSING UNIT | INDIAN INSTITUTE OF TECHNOLOGY, DELHI

- Designed and implemented an 8-core synthesizable GPGPU capable of FP16 and integer arithmetic
- integrated deeply pipelined FP units along with a SFU using Newton-Raphson and Goldschmidt methods
- Created LUT-based exponential/logarithmic hardware modules; verified functionality using OSS tools;
- synthesized the design using FreePDK45 and OpenROAD for architectural evaluation and optimized the system to clock at 500 MHz at 45 nm node.